AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor device comprising:

an insulating substrate having an interconnection pattern;

a solder resist;

a semiconductor element, having a projecting electrode, electrically connected to the interconnection pattern via the projecting electrode; and

a resin fillet for anchoring the semiconductor element,

said resin fillet being an insulating resin containing at least a resin anti-repellent for adjusting wettability of the insulating resin, and

wherein said solder resist is provided over part of the interconnection pattern but leaves the interconnection pattern exposed in an area that is to be connected to the semiconductor element via the projecting electrode, and wherein the insulating resin containing the anti-repellant covers at least edge portions of the solder resist, and wherein the solder resist is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above.

2. (Original) The semiconductor device as set forth in claim 1, wherein the resin anti-repellent improves wettability of the insulating resin for the interconnection pattern and the insulating substrate.

3. (Original) The semiconductor device as set forth in claim 1, wherein the insulating substrate is an insulating tape that is bendable.

4. (Original) The semiconductor device as set forth in claim 1, wherein the resin anti-repellent is a surfactant.

5. (Original) The semiconductor device as set forth in claim 1, wherein the insulating resin is a light curable resin or a thermosetting resin.

6. (Original) The semiconductor device as set forth in claim 1, wherein the insulating resin contains conductive particles dispersed in the insulating resin.

7. (Currently amended) A semiconductor device comprising:

an insulating substrate having an interconnection pattern;

a solder resist;

a semiconductor element, having a projecting electrode, electrically connected to the interconnection pattern via the projecting electrode; and

a resin fillet for anchoring the semiconductor element on the insulating substrate,

said resin fillet including an insulating resin, and a resin anti-repellent for improving wettability of the insulating resin for the interconnection pattern and the insulating substrate, and

wherein said solder resist is provided over part of the interconnection pattern but leaves the interconnection pattern exposed in an area that is to be connected to the semiconductor element via the projecting electrode, and wherein the insulating resin containing the anti-

repellant covers at least edge portions of the solder resist, and wherein the solder resist is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above.

8. (Withdrawn) A fabrication process of a semiconductor device, comprising the steps of:

(1) coating a solder resist on an interconnection pattern formed on an insulating substrate, except for a portion of the interconnection pattern where a semiconductor element is to be mounted;

(2) applying an insulating resin on a region including a portion where the semiconductor element is to be mounted, after said step (1); and

(3) placing the semiconductor element on the insulating resin, and pressing the semiconductor element against the interconnection pattern on the insulating substrate, so as to make an electrical connection between a projecting electrode of the semiconductor element and the interconnection pattern,

wherein the insulating resin used in said step (2) contains at least a resin anti-repellent for adjusting wettability of the insulating resin, and the insulating resin is applied in such a manner that a resin fillet is formed on side surfaces of the semiconductor element by a portion of the insulating resin pushed out from under the semiconductor element in said step (3) and by a portion of the insulating resin around the semiconductor element.

9. (Withdrawn) The fabrication process as set forth in claim 8, wherein the insulating substrate is an insulating tape that is bendable.

10. (Withdrawn) The fabrication process as set forth in claim 8, wherein, in said step (2), the insulating resin containing the resin anti-repellent is applied in such a manner that the insulating resin is in contact with the solder resist surrounding the insulating resin, or that the insulating resin partially covers the solder resist, or the insulating resin is applied in the vicinity of the solder resist to cover the solder resist by bleeding.

11. (Withdrawn) The fabrication process as set forth in claim 8, wherein, in said step (2), the insulating resin containing the resin anti-repellent is applied in such a manner that the insulating resin at least partially covers the solder resist, or the insulating resin is applied in the vicinity of the solder resist to cover the solder resist by bleeding.

12. (Withdrawn) The fabrication process as set forth in claim 8, wherein the resin anti-repellent is a surfactant.

13. (Withdrawn) The fabrication process as set forth in claim 8, wherein the insulating resin is a light curable resin or a thermosetting resin.

14. (Withdrawn) The fabrication process as set forth in claim 8, wherein the insulating resin contains conductive particles dispersed in the insulating resin.

15. (Currently amended) A semiconductor device comprising:

an insulating substrate having an interconnection pattern;

a solder resist;

a semiconductor element, having a projecting electrode, electrically connected to the interconnection pattern via the projecting electrode; and

a resin fillet for anchoring the semiconductor element,

said resin fillet being an insulating resin containing at least a resin anti-repellent for adjusting wettability of the insulating resin, and

said solder resist coating the interconnection pattern except for an area that is connected to the semiconductor element via the projecting electrode,

said resin fillet covering edge portions of the solder resist so that the interconnection pattern is not made exposed in an area that is not covered with the solder resist, and

wherein the solder resist is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above.

16. (Currently amended) A semiconductor device comprising:

an insulating substrate having an interconnection pattern;

a solder resist;

a semiconductor element, having a projecting electrode, electrically connected to the interconnection pattern via the projecting electrode; and

a resin fillet for anchoring the semiconductor element on the insulating substrate,

said resin fillet including an insulating resin, and a resin anti-repellent for improving wettability of the insulating resin for the interconnection pattern and the insulating substrate,

said solder resist coating the interconnection pattern except for an area that is connected to the semiconductor element via the projecting electrode,

the insulating resin containing the resin anti-repellant covering edge portions of the solder resist so that the interconnection pattern is not made exposed in an area that is not covered with the solder resist, and

wherein the solder resist is laterally offset and spaced laterally outwardly from an outer edge of the semiconductor element when viewed from above.